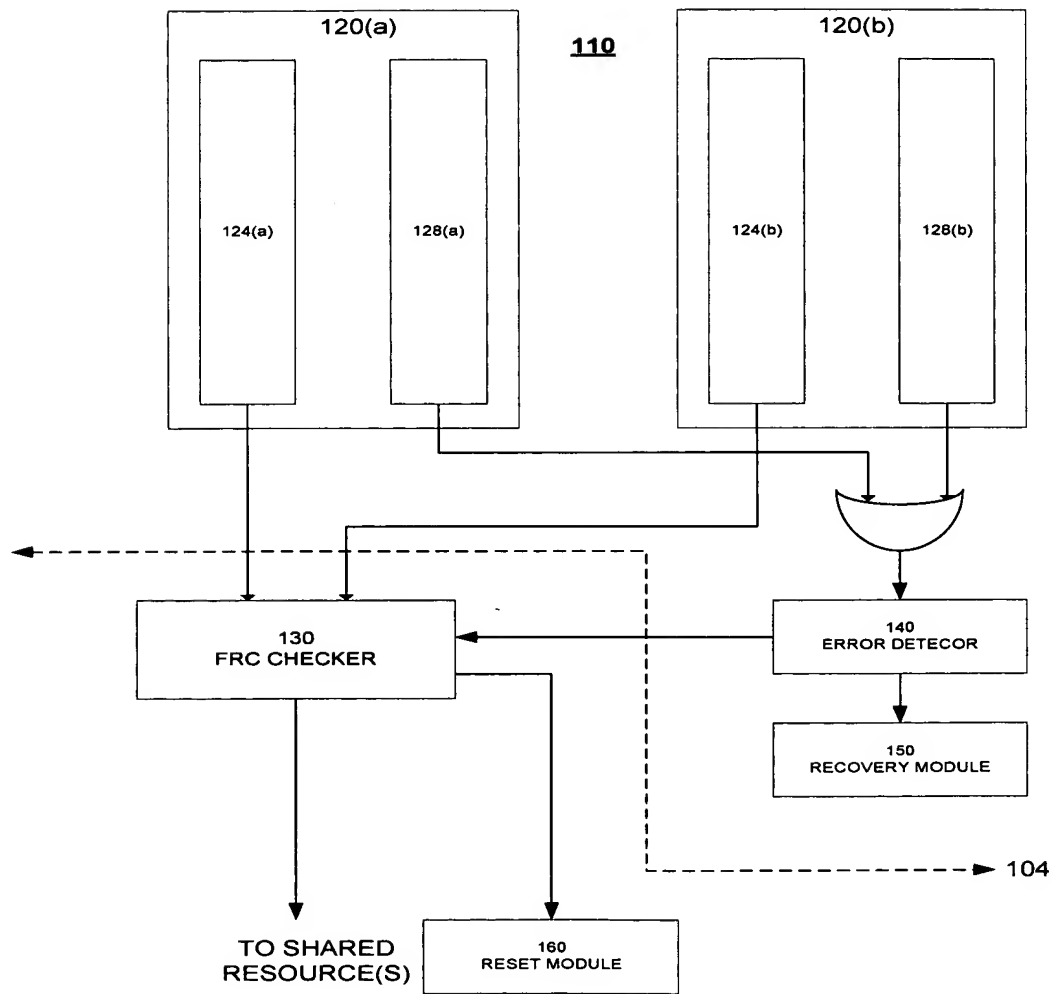




Replacement Sheet



PRIOR ART

Fig. 1



Replacement Sheet

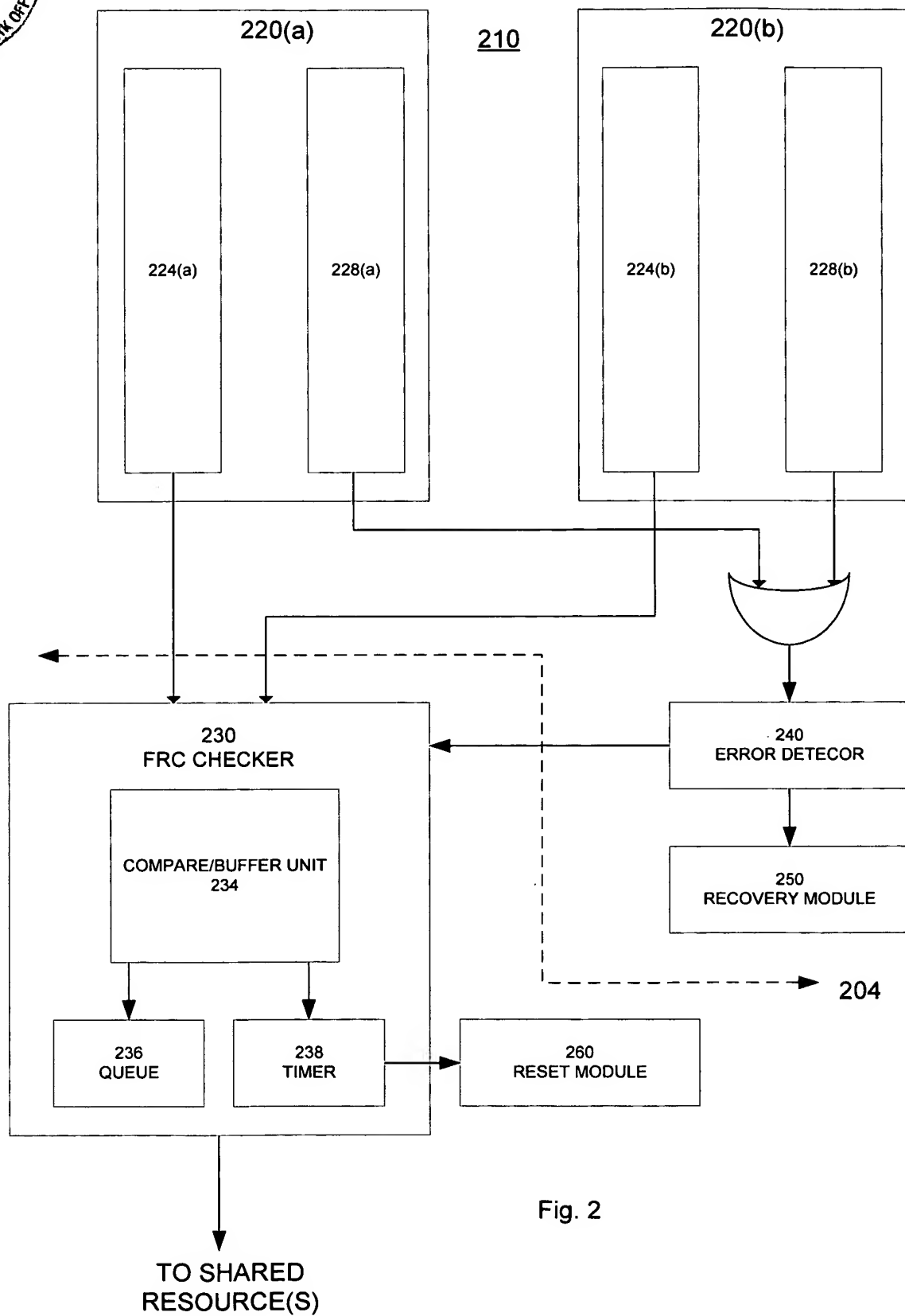


Fig. 2



Replacement Sheet

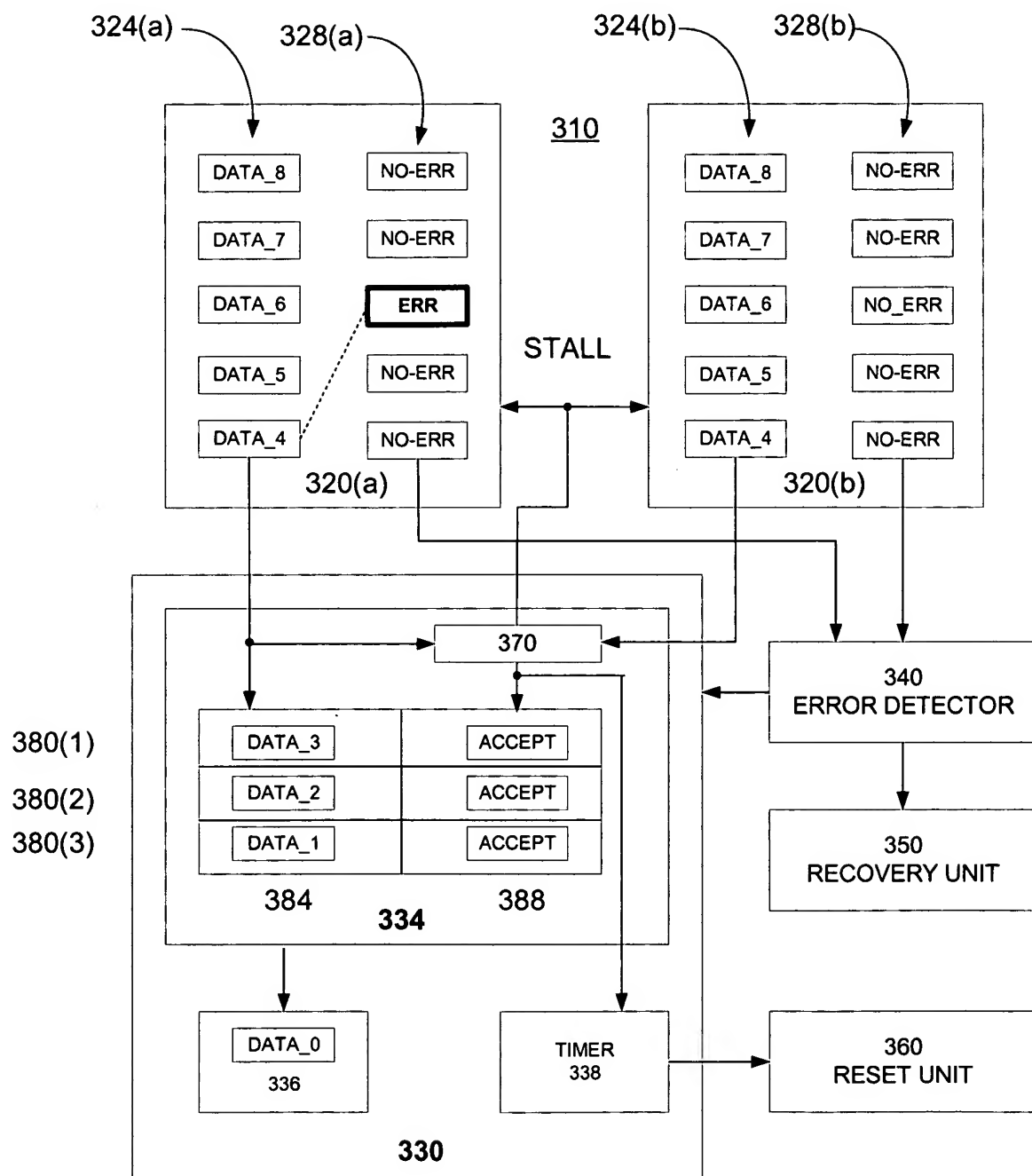


Fig. 3A

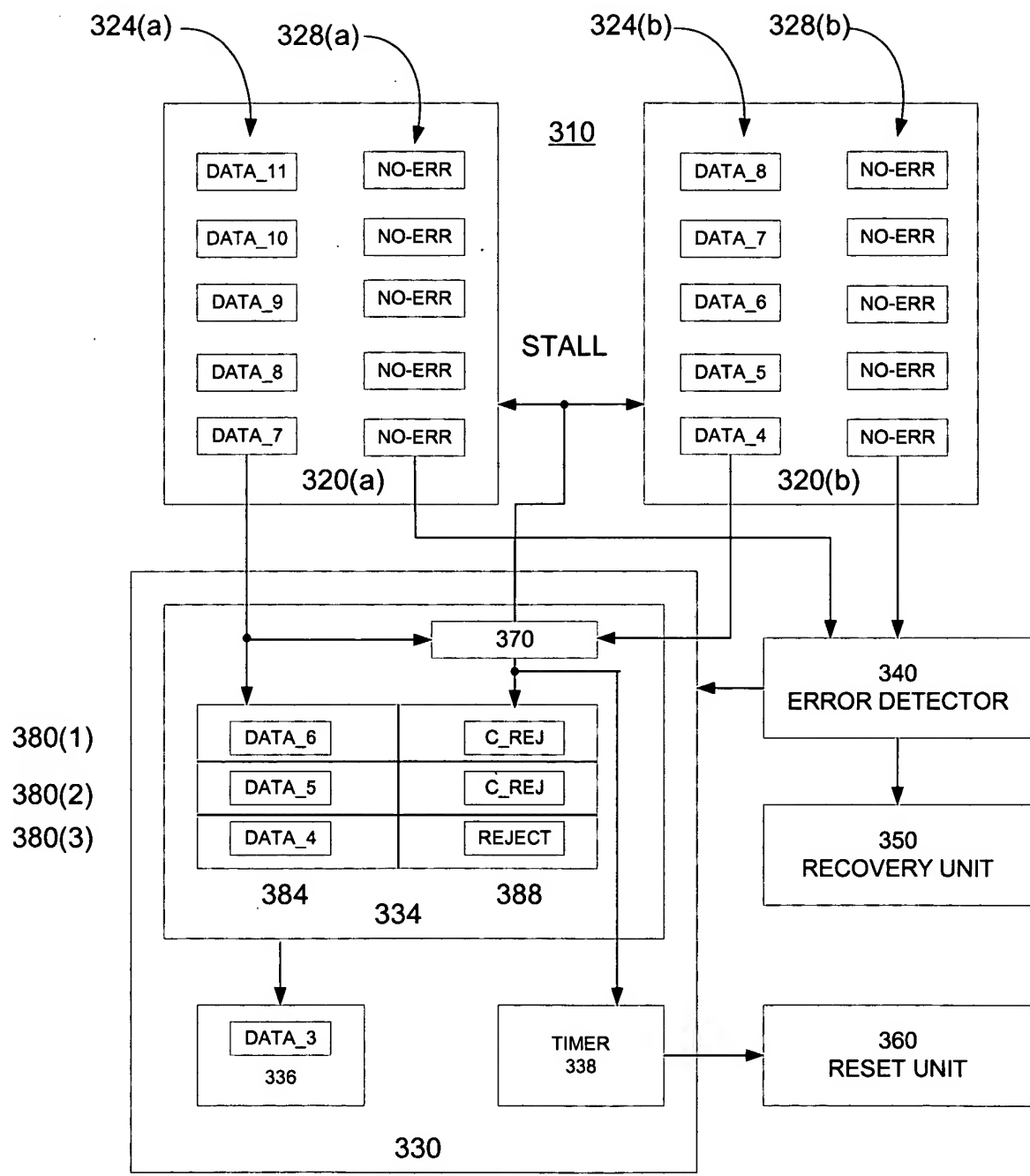


Fig. 3B



Replacement Sheet

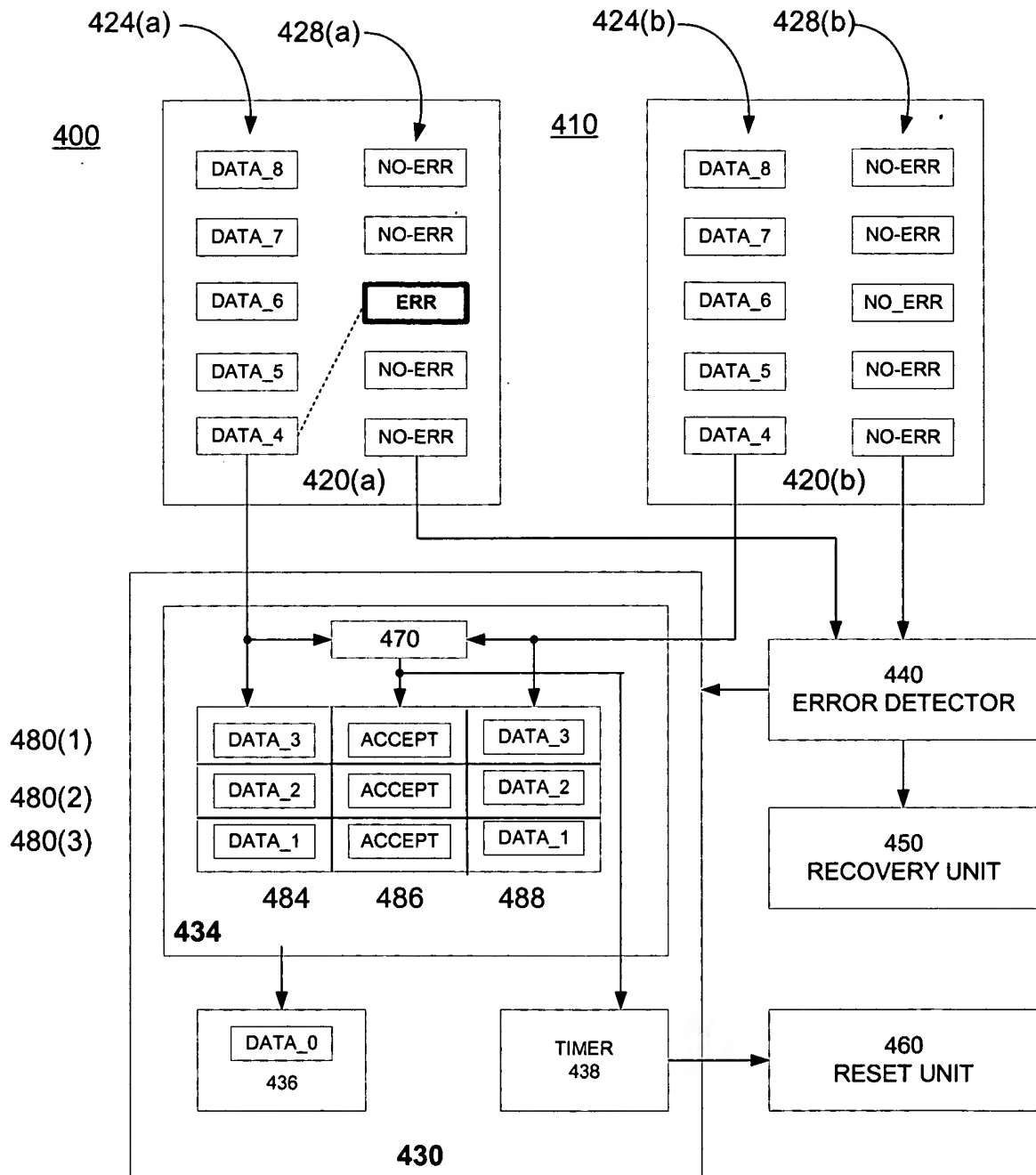
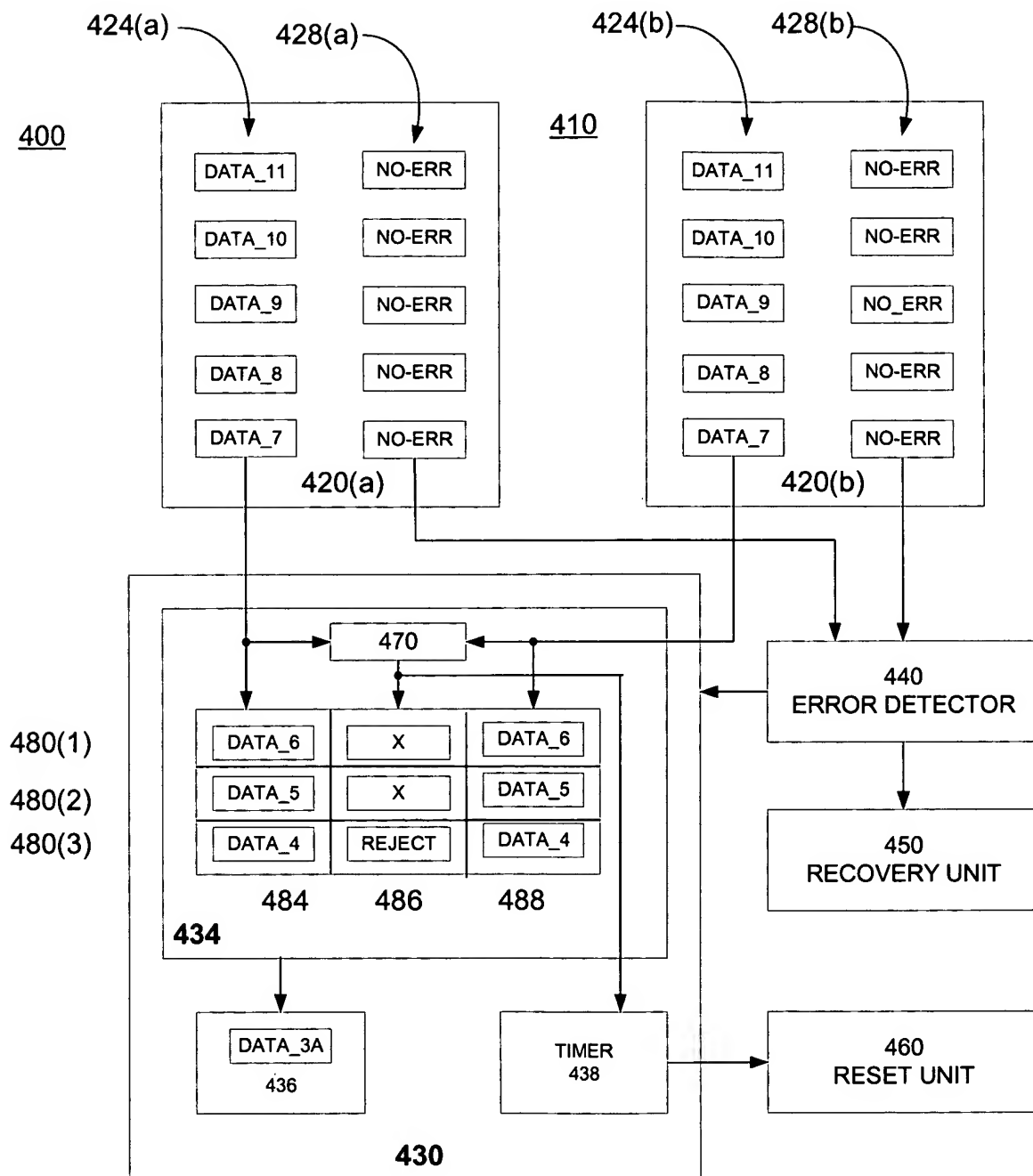


Fig. 4A





Replacement Sheet

500

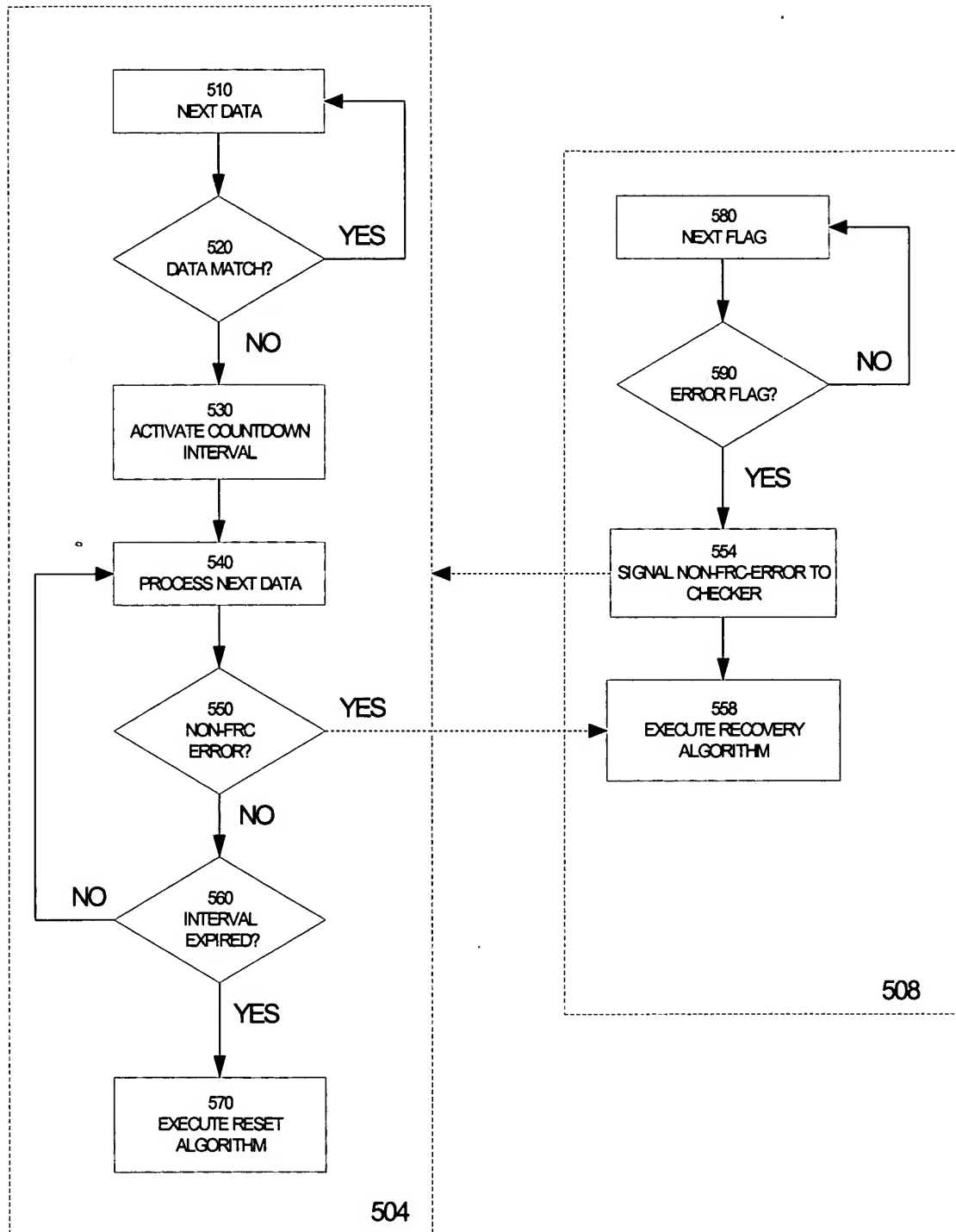


Fig. 5

Figure 600 is a block diagram of a system architecture. At the top, a box labeled "NON-VOLATILE MEMORY 690" contains sub-components 692 and 694. Below it, a box labeled "PERIPHERAL DEVICES 698" is connected to a central "CHIPSET 682". To the right, a box labeled "MAIN MEMORY 680" also contains sub-components 692 and 694 and is connected to the chipset. A large double-headed arrow labeled "FSB 660" (Front Side Bus) connects the chipset to the lower part of the diagram. On the left, a "SNOOP BLOCK 662" is connected to the FSB and an "XOR 666" block. In the center, a "L3 CACHE 640" is connected to an "ERROR CHECKER/ DETECTOR 630(a)". To the right of the cache is another "ERROR CHECKER/ DETECTOR 630(b)". Below these are two "BUS CLUSTER" blocks, 628(a) and 628(b). At the bottom are two "EXECUTION RESOURCES" blocks, 624(a) and 624(b). On the far right, there are two interrupt controller blocks, 670(b) and 670(a), each containing "INT_C 678(b)" and "INT_C 674(b)" and "INT_C 678(a)" and "INT_C 674(a)" respectively, connected by an "XOR 672" block. Various lines and arrows indicate data and control flow between these components, including a dashed line labeled 664 separating the error checker/detector blocks from the interrupt controllers.